

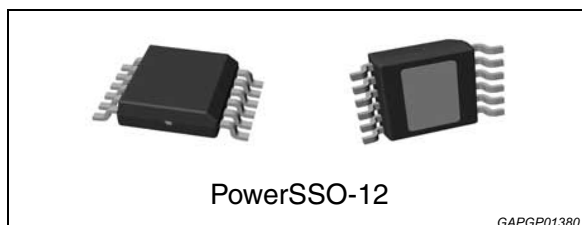
## 5 V low dropout voltage regulator

### Features

Max DC supply voltage	$V_S$	40 V
Max output voltage tolerance	$\Delta V_O$	+/-2%
Max dropout voltage	$V_{dp}$	500 mV
Output current	$I_O$	150 mA
Quiescent current	$I_{qn}$	5 $\mu A^{(1)}$ 55 $\mu A^{(2)}$

1. Typical value with regulator disabled.
2. Typical value with regulator enabled.

- Operating DC supply voltage range 5.6 V to 40 V
- Low dropout voltage
- Low quiescent current consumption
- Precision output voltage 5 V +/- 2%
- Reset circuit sensing the output voltage
- Programmable reset pulse delay with external capacitor
- Adjustable reset threshold
- Early warning
- Very wide stability range with low value output capacitor
- Thermal shutdown and short-circuit protection
- Wide temperature range ( $T_j = -40\text{ }^{\circ}\text{C}$  to  $150\text{ }^{\circ}\text{C}$ )
- Enable input for enabling / disabling the voltage regulator



### Description

L5150GJ is a low dropout linear regulator with microprocessor control functions such as power on reset, low voltage reset, early warning, on/off control. Typical quiescent current is 55  $\mu A$  in very low output current mode and enabled regulator. It drops to 5  $\mu A$  with not enabled regulator.

On chip trimming results in high output voltage accuracy (2%). Accuracy is kept over wide temperature range, line and load variation. Early warning circuit monitors the input voltage and compares it to an internal voltage reference.

Output voltage reset threshold can be adjusted down to 3.5 V by means of an external voltage divider.

The maximum input voltage is 40 V. The max output current is internally limited. Internal temperature protection disables the voltage regulator output. In addition, only low-value ceramic capacitor on output is required for stability.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape & reel
PowerSSO-12	L5150GJ	L5150GJTR

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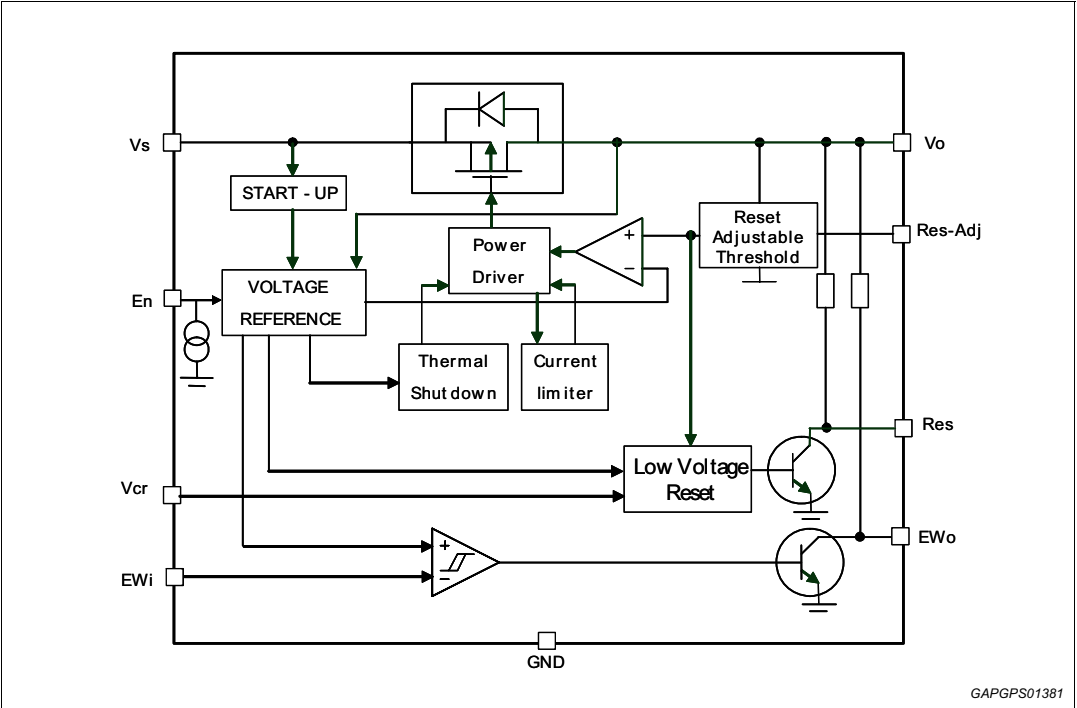
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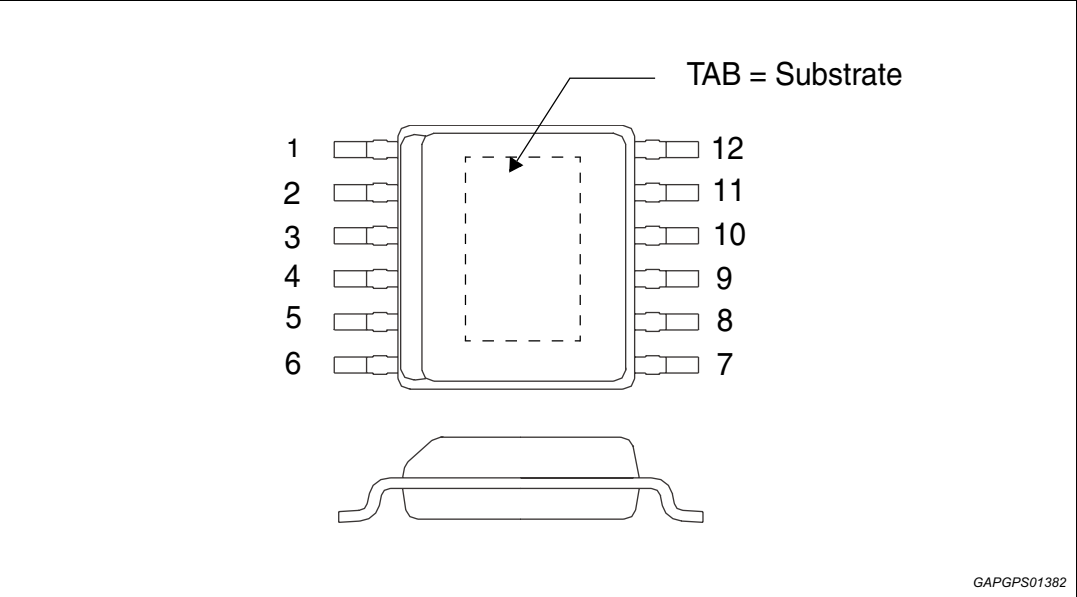
# 1 Block diagram and pins description

Figure 1. Block diagram



GAPGPS01381

Figure 2. Configuration diagram (top view)



GAPGPS01382

**Table 2. Pins description**

Pin	Name	Function
1	$R_{es\_Adj}$	Reset adjustable threshold. Connected to an appropriate external voltage divider, it allows to properly set the reset threshold down to 3.5 V. Connect to GND if not needed.
2	$R_{es}$	Reset output. Internally connected to $V_o$ through a 20 K $\Omega$ pull-up resistor. This pin is pulled low when $V_o < V_{o\_th}$ . Keep open if not needed.
3	$V_{cr}$	Reset delay. Connect an external capacitor between $V_{cr}$ pin and ground to adjust the reset delay time. Keep open if not needed.
4	GND	Ground reference.
5	NC	Not connected.
6	$V_o$	5 V regulated output. Block to GND with a ceramic capacitor ( $C_o \geq 220$ nF for regulator stability).
7	$V_S$	Supply voltage, block directly to GND on the IC with a capacitor.
8	NC	Not connected.
9	$E_n$	Enable input. A high signal switches the regulator on. Connect to $V_S$ if not needed.
10	$EW_i$	Early warning input. This pin monitors the $V_S$ voltage level through a resistor divider. Connect to $V_S$ if not needed.
11	NC	Not connected.
12	$EW_o$	Early warning output. Internally connected to $V_o$ through 20 K $\Omega$ pull up resistor. This pin is pulled low when $EW_i$ is below bandgap reference voltage. Keep open if not needed.
-	TAB	TAB is connected to the substrate of the chip: connect to GND or leave open (see <a href="#">Figure 2</a> ).

## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Stressing the device above the rating listed in the [Table 3: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality documents.

**Table 3. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{sdc}$	DC supply voltage	-0.3 to 40	V
$I_{sdc}$	Input current	Internally limited	
$V_{odc}$	DC output voltage	-0.3 to 6	V
$I_{odc}$	DC output current	Internally limited	
$V_{od\ Res}$	Open drain output voltage $R_{es}$	-0.3 to $V_{odc} + 0.3$	V
$I_{od\ Res}$	Open drain output current $R_{es}$	Internally limited	
$V_{Res\_adj}$	$V_{Res\_adj}$ voltage	-0.3 to $V_{odc} + 0.3$	V
$V_{od\ EW0}$	Open drain output voltage $EW_0$	-0.3 to $V_{odc} + 0.3$	V
$I_{od\ EW0}$	Open drain output current $EW_0$	Internally limited	
$V_{cr}$	$V_{cr}$ voltage	-0.3 to $V_o + 0.3$	V
$V_{EWi}$	Early warning input voltage	-0.3 to 40	V
$V_{En}$	Enable input	-0.3 to 40	V
$T_j$	Junction temperature	-40 to 150	°C
VESD HBM	ESD HBM voltage level (HBM-MIL STD 883C)	+/- 2	kV
VESD CDM	ESD CDM voltage level (CDM- )	+/- 750	V

### 2.2 Thermal data

**Table 4. Thermal data<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction to case: PowerSSO-12	20	°K/W
$R_{thj-amb}$	Thermal resistance junction to ambient: PowerSSO-12	52	°K/W

1. The values quoted are for PCB 77 mm x 86 mm x 1.6 mm, FR4, double copper layer with single heatsink layer, copper thickness 70 µm, thermal vias, copper area 2 cm<sup>2</sup>.

## 2.3 Electrical characteristics

Values specified in this section are for  $V_S = 5.6 \text{ V}$  to  $31 \text{ V}$ ,  $T_j = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$  unless otherwise stated.

**Table 5. General**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_O$	$V_{O\_ref}$	Output voltage	$V_S = 8 \text{ V}$ to $18 \text{ V}$ , $I_O = 8 \text{ mA}$ to $150 \text{ mA}$	4.9	5.0	5.1	V
$V_O$	$V_{O\_ref}$	Output voltage	$V_S = 5.6 \text{ V}$ to $31 \text{ V}$ , $I_O = 8 \text{ mA}$ to $150 \text{ mA}$	4.85	5.0	5.15	V
$V_O$	$V_{O\_ref}$	Output voltage	$V_S = 5.6 \text{ V}$ to $31 \text{ V}$ , $I_O = 0.1 \text{ mA}$ to $8 \text{ mA}$	4.75	5.0	5.25	V
$V_O$	$I_{short}$	Short-circuit current	$V_S = 13.5 \text{ V}$	0.65	0.95	1.25	A
$V_O$	$I_{lim}$	Output current capability <sup>(1)</sup>	$V_S = 13.5 \text{ V}$	280	470	660	mA
$V_S, V_O$	$V_{line}$	Line regulation voltage	$V_S = 6 \text{ V}$ to $28 \text{ V}$ , $I_O = 30 \text{ mA}$			40	mV
$V_O$	$V_{load}$	Load regulation voltage	$V_S = 8 \text{ V}$ to $18 \text{ V}$ , $I_O = 8 \text{ mA}$ to $150 \text{ mA}$			55	mV
			$V_S = 13.5 \text{ V}$ , $T_j = 25 \text{ }^\circ\text{C}$ , $I_O = 8 \text{ mA}$ to $150 \text{ mA}$			40	
$V_S, V_O$	$V_{dp}$	Drop voltage <sup>(2)</sup>	$I_O = 150 \text{ mA}$			500	mV
$V_S, V_O$	SVR	Ripple rejection	$f_r = 100 \text{ Hz}$ <sup>(3)</sup>		60		dB
$V_O$	$I_{oth\_H}$	Normal consumption mode output current	$V_S = 8 \text{ V}$ to $18 \text{ V}$	8			mA
$V_O$	$I_{oth\_L}$	Very low consumption mode output current	$V_S = 8 \text{ V}$ to $18 \text{ V}$			1.1	mA
$V_O$	$I_{oth\_Hyst}$	Output current switching threshold hysteresis	$V_S = 13.5 \text{ V}$ , $T_j = 25 \text{ }^\circ\text{C}$		0.8		mA
$V_S, V_O$	$I_{qs}$	Current consumption with regulator disabled $I_{qs} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$ , $E_n = \text{low}$		5	10	$\mu\text{A}$
$V_S, V_O$	$I_{qn\_1}$	Current consumption with regulator enabled $I_{qn\_1} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$ , $I_O = 0.1 \text{ mA}$ to $1 \text{ mA}$ , $E_n = \text{high}$ $T_j = 25 \text{ }^\circ\text{C}$		55	80	$\mu\text{A}$
			$V_S = 13.5 \text{ V}$ , $I_O = 0.1 \text{ mA}$ to $1 \text{ mA}$ , $E_n = \text{high}$			95	
$V_S, V_O$	$I_{qn\_150}$	Current consumption with regulator enabled $I_{qn\_150} = I_{VS} - I_O$	$V_S = 13.5 \text{ V}$ , $I_O = 150 \text{ mA}$ , $E_n = \text{high}$		3.2	4.2	mA



**Table 5. General (continued)**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	$T_w$	Thermal protection temperature		150		190	°C
	$T_{w\_hy}$	Thermal protection temperature hysteresis			10		°C

1. Measured output current when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and  $I_o = 75$  mA.
2.  $V_s - V_o$  measured dropout when the output voltage has dropped 100 mV from its nominal value obtained at 13.5 V and  $I_o = 75$  mA.
3. Guaranteed by design.

**Table 6. Reset**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$R_{es}$	$V_{res\_l}$	Reset output low voltage	$R_{ext} = 5$ kW, $V_o > 1$ V			0.4	V
$R_{es}$	$I_{Res\_lkg}$	Reset output high leakage current	$V_{Res} = 5$ V			1	μA
$R_{es}$	$R_{Res}$	Pull up internal resistance	Versus $V_o$	10	20	40	kΩ
$R_{es}$	$V_{o\_th}$	$V_o$ out of regulation threshold	$V_{Res\_adj} < 0.2$ V, $V_o$ decreasing	6	8	10	% Below $V_{o\_ref}$
$R_{es\_adj}$	$V_{Res\_adj}$	Reset adjustable switching threshold		2.35	2.5	2.65	V
$R_{es\_adj}$	$V_{Res\_adjl}$	Reset adjustable low voltage		0.4	0.9	1.3	V
$R_{es\_adj}$	$I_{Res\_adj\_lkg}$	Reset adjustable leakage current	$V_{Res\_adj} = 2.5$ V	-1		1	μA
$V_{cr}$	$V_{Rlth}$	Reset timing low threshold	$V_S = 13.5$ V	15	18	22	% $V_{o\_ref}$
$V_{cr}$	$V_{Rhth}$	Reset timing high threshold	$V_S = 13.5$ V	47	50	53	% $V_{o\_ref}$
$V_{cr}$	$I_{cr}$	Charge current	$V_S = 13.5$ V	10	20	30	μA
$V_{cr}$	$I_{dr}$	Discharge current	$V_S = 13.5$ V	10	20	30	μA
$R_{es}$	$T_{rr}$	Reset reaction time				2	μs
$R_{es}$	$T_{rd}$	Reset delay time	$V_S = 13.5$ V, $C_{tr} = 1000$ pF	2	4	6	ms

**Table 7. Early warning**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E <sub>Wi</sub>	V <sub>EWi_thl</sub>	EW input low threshold voltage		2.35	2.50	2.65	V
EW <sub>i</sub>	V <sub>EWi_thh</sub>	EW input high threshold voltage		2.42	2.57	2.72	V
EW <sub>i</sub>	V <sub>EWi_thhyst</sub>	EW input threshold hysteresis			70		mV
EW <sub>i</sub>	I <sub>EWi_lkg</sub>	EW input leakage current	V <sub>EWi</sub> = 2.5 V, V <sub>S</sub> > 4 V	-1		1	μA
EW <sub>o</sub>	R <sub>EWo</sub>	Pull up internal resistance	Versus V <sub>o</sub>	10	20	40	kΩ
EW <sub>o</sub>	V <sub>EWo_lv</sub>	EW output low voltage (with external pull up)	V <sub>EWi</sub> < 2.35 V, V <sub>S</sub> > 4 V, R <sub>ext</sub> = 5 kΩ			0.4	V
EW <sub>o</sub>	I <sub>EWo_lkg</sub>	EW output leakage current	V <sub>EWo</sub> = 5 V			1	μA

**Table 8. Enable**

Pin	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E <sub>n</sub>	V <sub>En_low</sub>	E <sub>n</sub> input low voltage				1	V
E <sub>n</sub>	V <sub>En_high</sub>	E <sub>n</sub> input high voltage		3			V
E <sub>n</sub>	V <sub>En_hyst</sub>	E <sub>n</sub> input hysteresis			500		mV
E <sub>n</sub>	I <sub>_leak</sub>	Pull-down current	V <sub>En</sub> = 5 V		1.8	10	μA

## 2.4 Electrical characteristics curves

Figure 3. Output voltage vs.  $T_j$

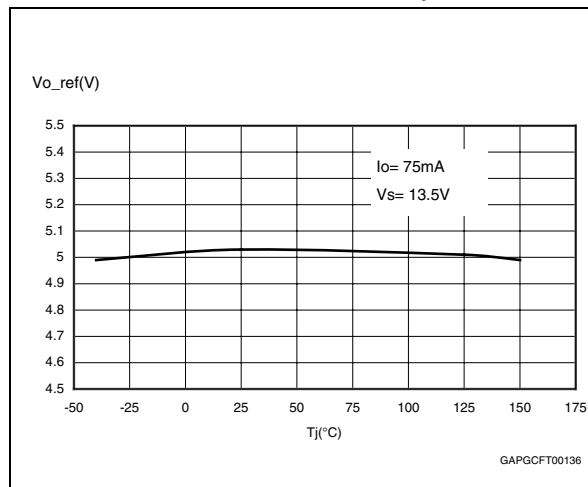


Figure 4. Output voltage vs.  $V_s$

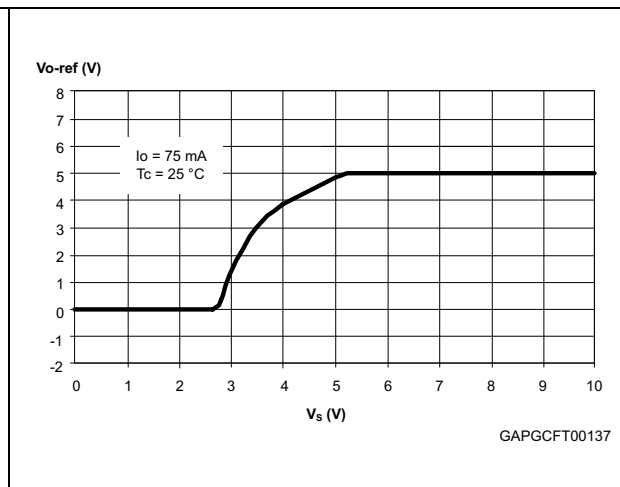


Figure 5. Output voltage vs.  $V_{En}$

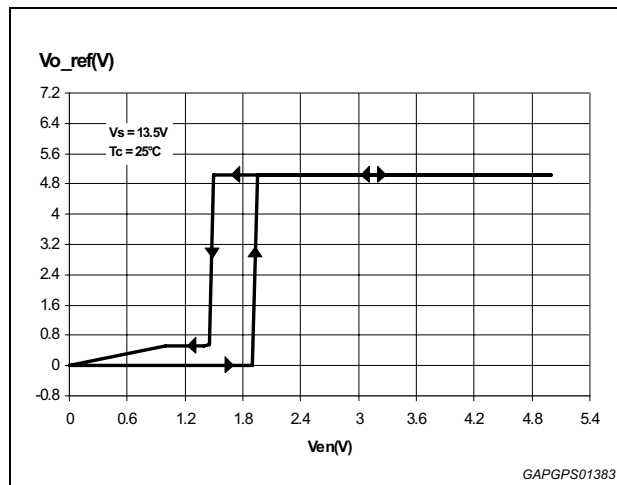


Figure 6. Drop voltage vs. output current

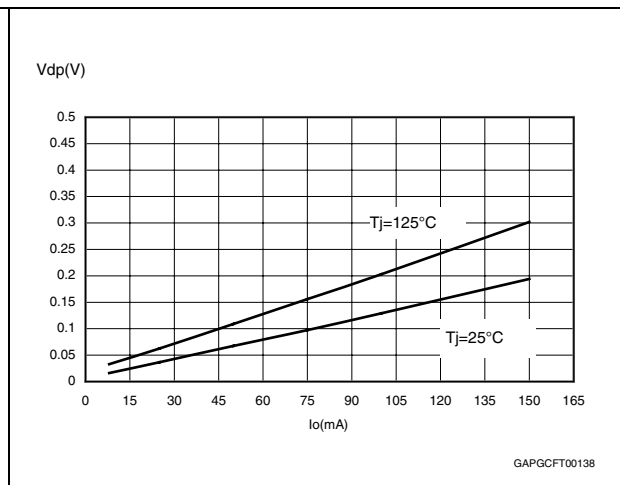


Figure 7. Current consumption vs. output current

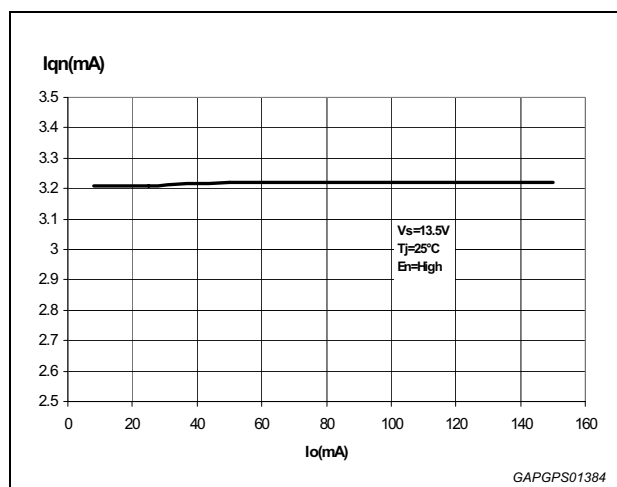


Figure 8. Current consumption vs. output current (at light load condition)

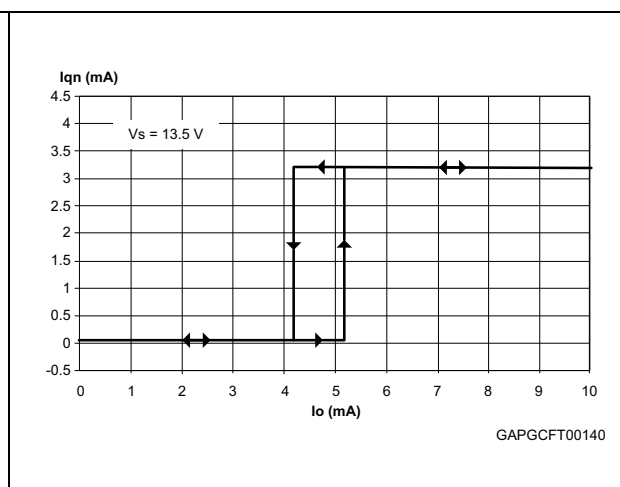


Figure 9. Current consumption vs. input voltage ( $I_o = 0.1\text{ mA}$ )

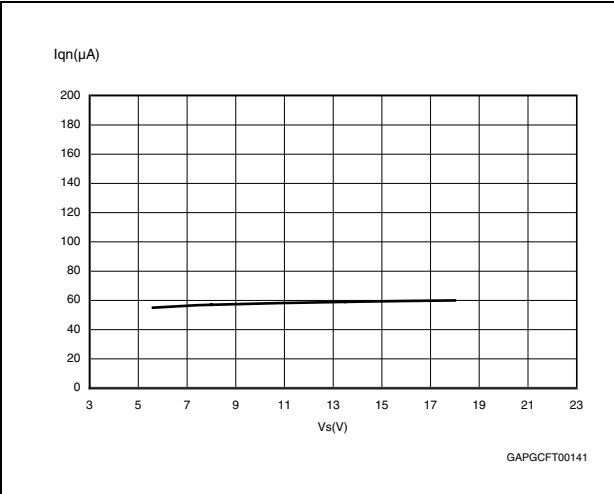


Figure 10. Current consumption vs. input voltage ( $I_o = 75\text{ mA}$ )

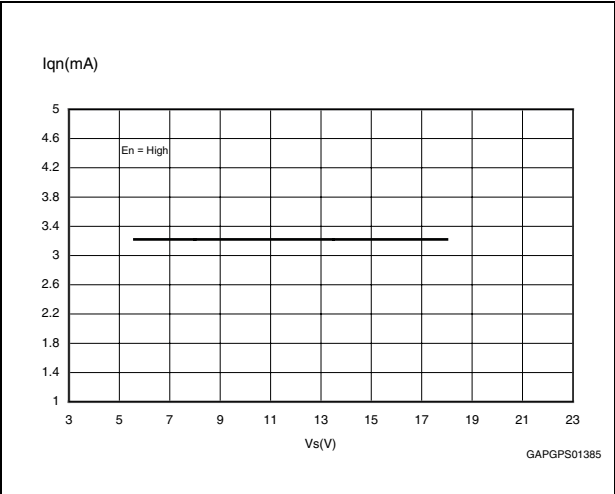


Figure 11. Current limitation vs.  $T_j$

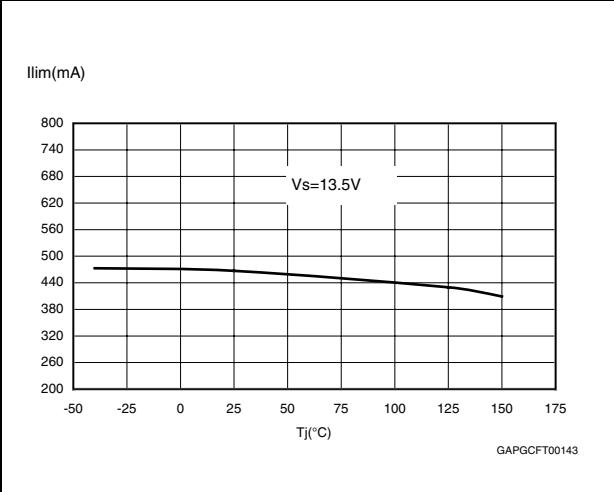


Figure 12. Current limitation vs. input voltage

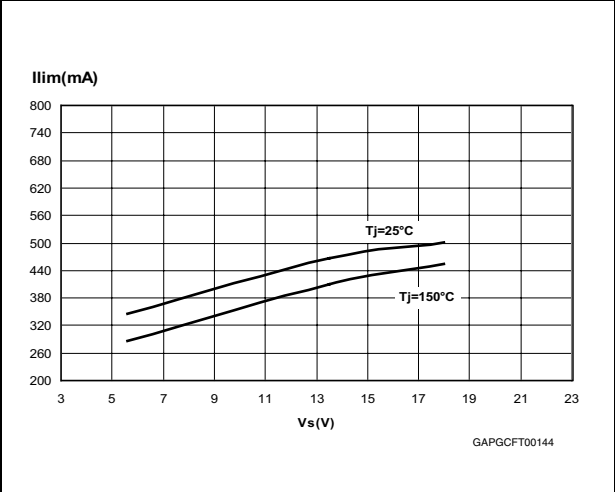


Figure 13. Short-circuit current vs.  $T_j$

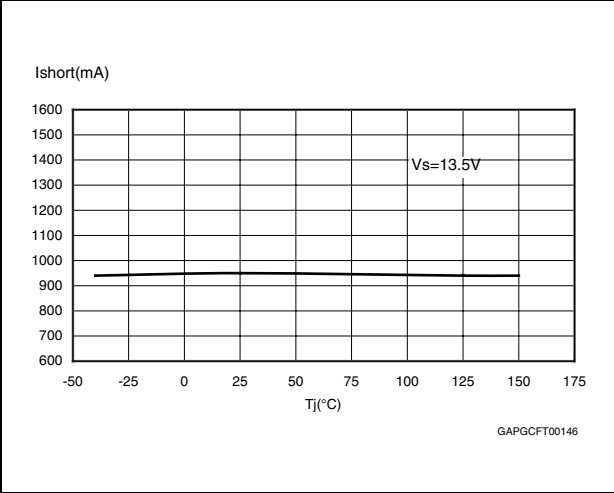


Figure 14. Short-circuit current vs. input voltage

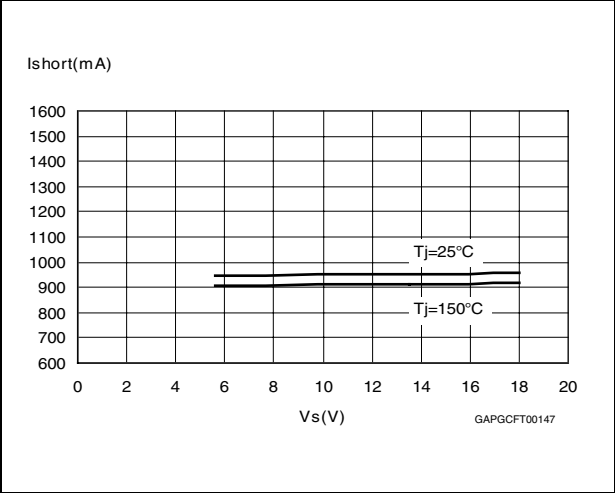


Figure 15.  $V_{En\_high}$  vs.  $T_j$

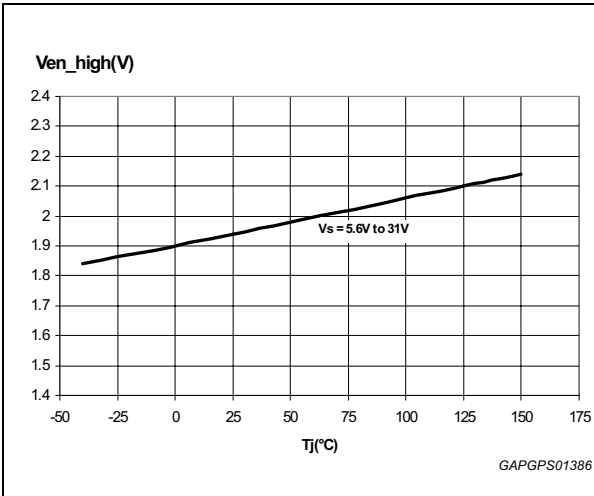


Figure 16.  $V_{En\_low}$  vs.  $T_j$

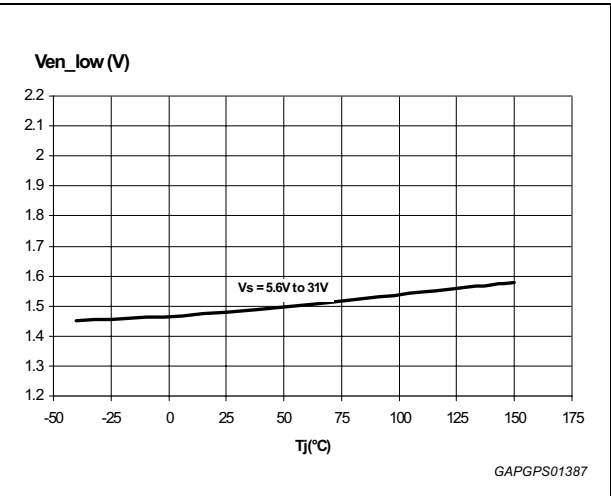


Figure 17.  $V_{Rthh}$  vs.  $T_j$

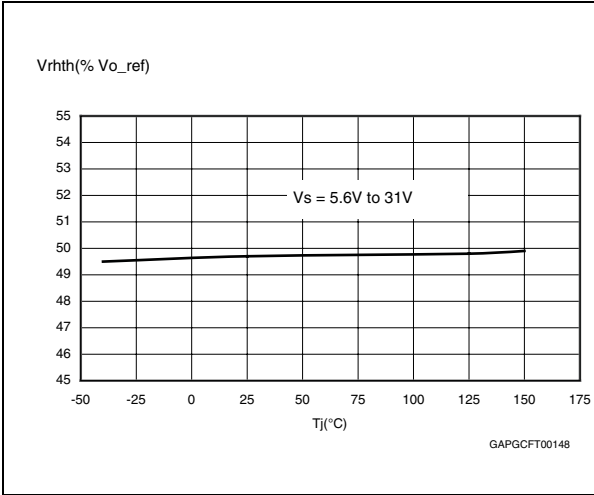


Figure 18.  $V_{Rlth}$  vs.  $T_j$

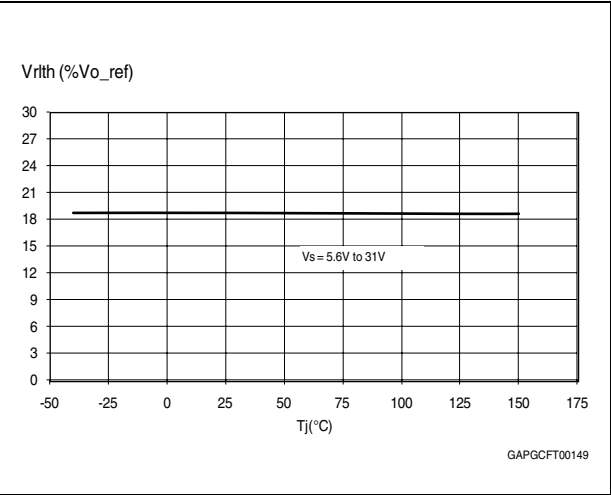


Figure 19.  $V_{EWi\_thh}$  vs.  $T_j$

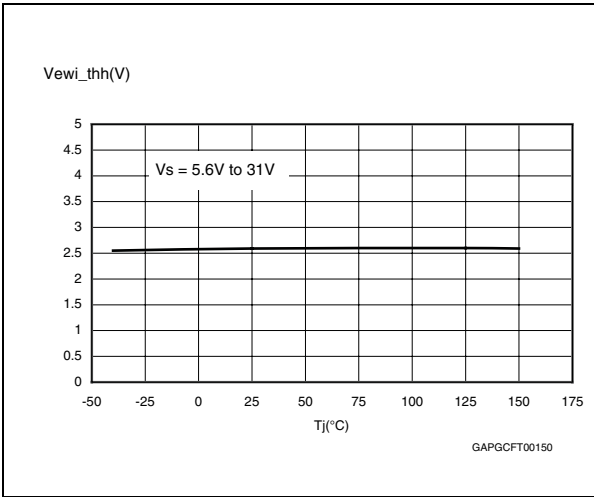


Figure 20.  $V_{EWi\_thl}$  vs.  $T_j$

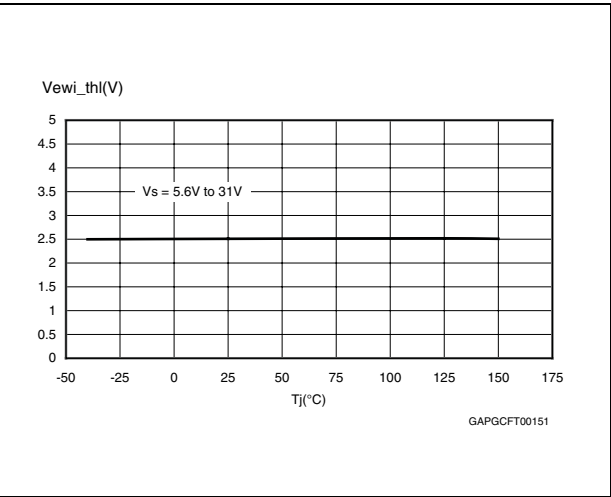


Figure 21.  $I_{cr}$  vs.  $T_j$

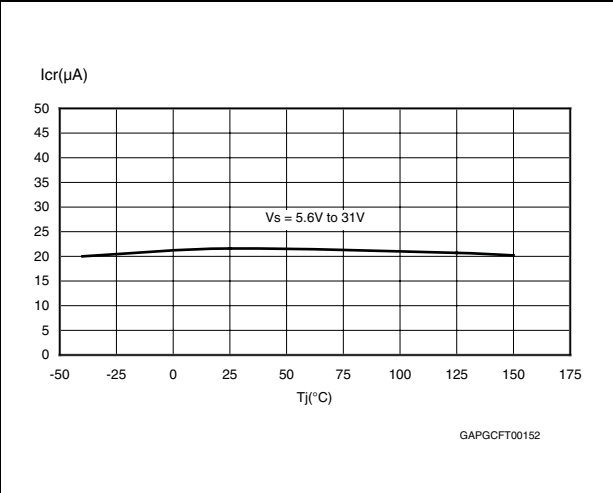


Figure 22.  $I_{dr}$  vs.  $T_j$

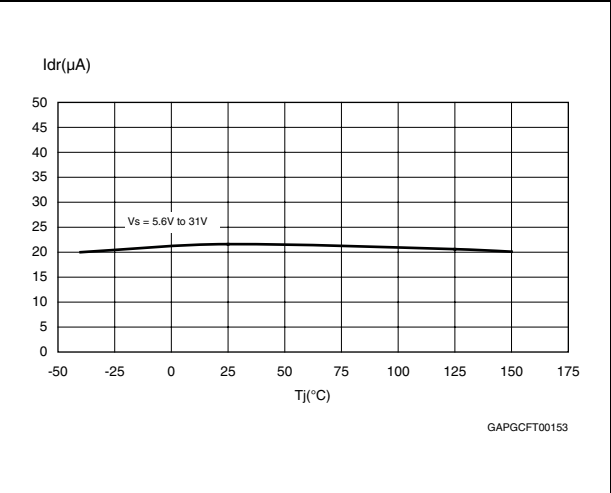
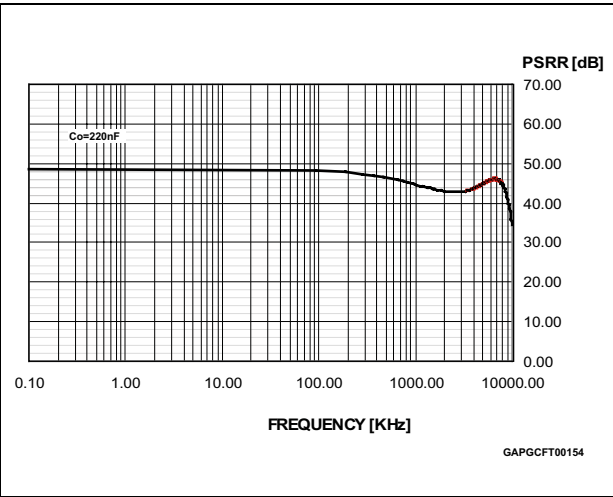


Figure 23. PSRR

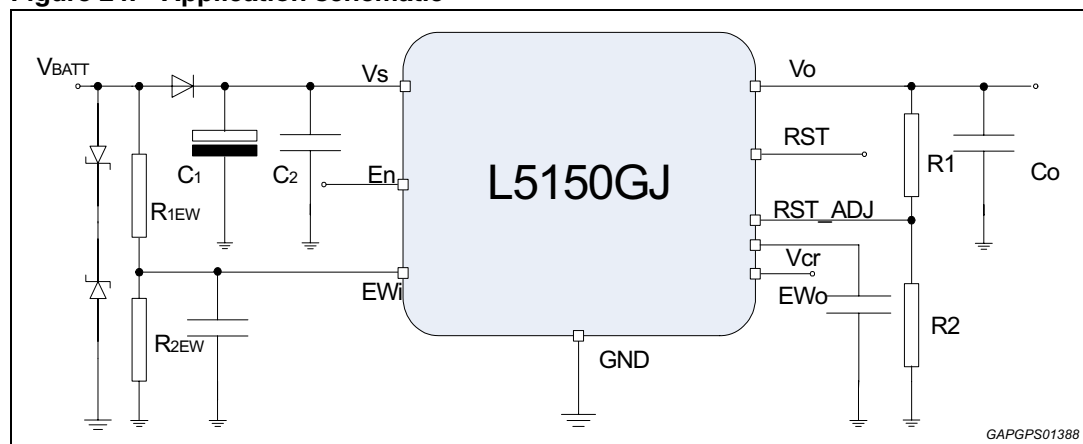


### 3 Application information

### 3.1 Voltage regulator

The voltage regulator uses a p-channel mos transistor as a regulating element. With this structure a very low dropout voltage at current up to 150 mA is obtained. The output voltage is regulated up to input supply voltage of 40 V. The high-precision of the output voltage (2%) is obtained with a pre-trimmed reference voltage. The voltage regulator automatically adapts its own quiescent current to the output current level. In light load conditions the quiescent current goes down to 55  $\mu$ A only (low consumption mode). This procedure features a certain hysteresis on the output current (see [Figure 8](#)). Short-circuit protection to GND and a thermal shutdown are provided.

**Figure 24. Application schematic**



The input capacitor  $C_1 \geq 100 \mu\text{F}$  is necessary as backup supply for negative pulses which may occur on the line. The second input capacitor  $C_2 \geq 220 \text{ nF}$  is needed when the  $C_1$  is too distant from the  $V_S$  pin and it compensates smooth line disturbances. The  $C_0$  ceramic capacitor, connected to the output pin, is for bypassing to GND the high-frequency noise and it guarantees stability even during sudden line and load variations. Suggested value is  $C_0 = 220 \text{ nF}$  with  $\text{ESR} \geq 100 \text{ m}\Omega$ .

Stability region is reported in *Figure 25*.

Figure 25. Stability region

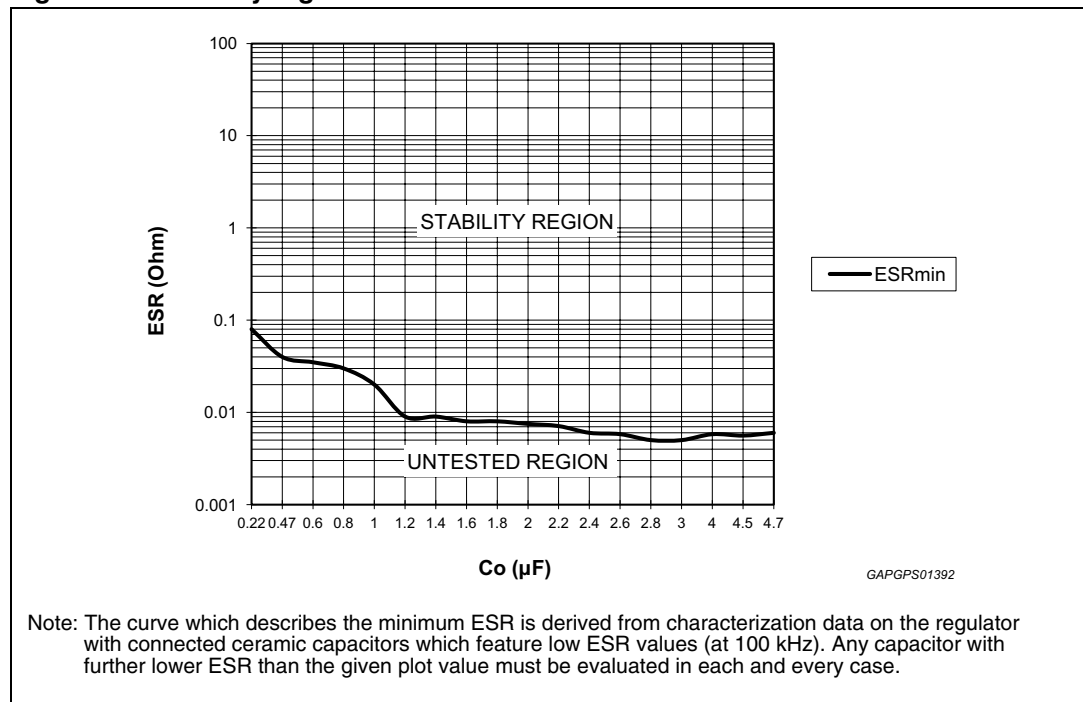
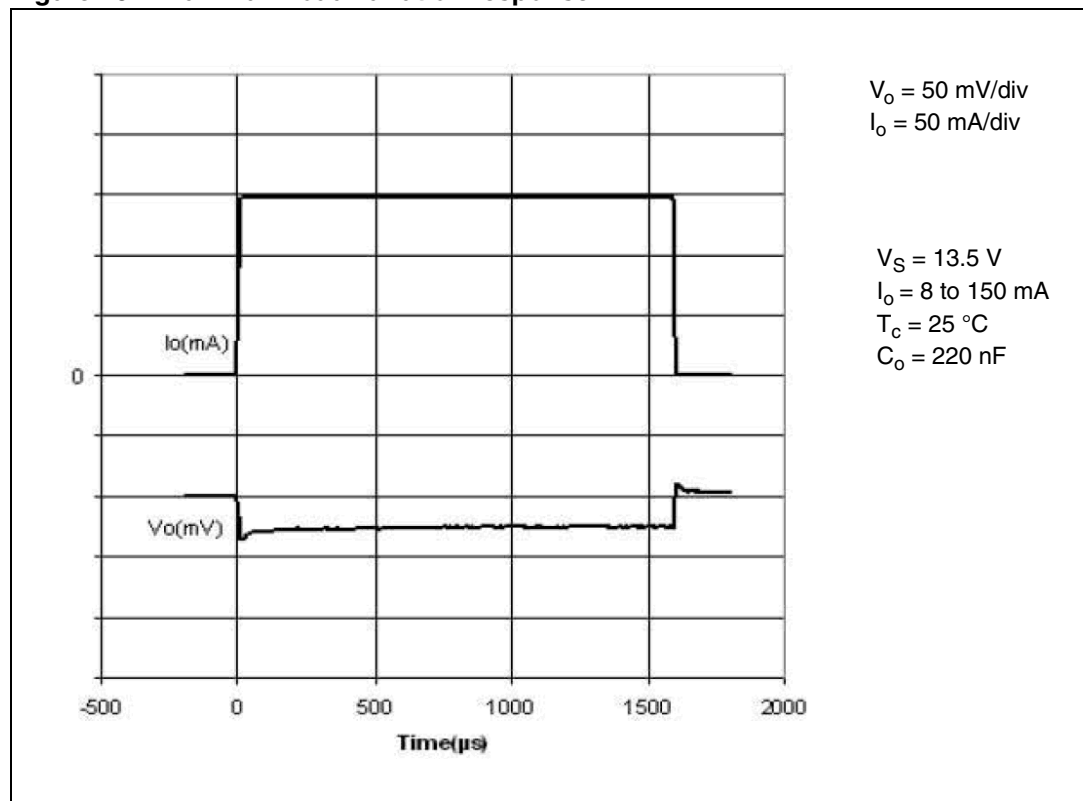


Figure 26. Maximum load variation response





### 3.2 Reset

The reset circuit monitors the output voltage  $V_o$ . If the output voltage becomes lower than  $V_{o\_th}$  then  $R_{es}$  goes low with a delay time ( $t_{rr}$ ). When the output voltage becomes higher than  $V_{o\_th}$  then  $R_{es}$  goes high with a delay time  $t_{rd}$ . This delay is obtained by 32 periods of oscillator.

The oscillator period is given by:

#### Equation 1

$$T_{osc} = [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{cr} + [(V_{Rhth} - V_{Rlth}) \times C_{tr}] / I_{dr}$$

where:

$I_{cr}$  = 20  $\mu$ A is an internally generated charge current,

$I_{dr}$  = 20  $\mu$ A is an internally generated discharge current,

$V_{Rhth}$  = 2.5 V (typ) and  $V_{Rlth}$  = 0.9 V (typ) are two voltage thresholds,

$C_{tr}$  is an external capacitor put between  $V_{cr}$  pin and GND.

Reset pulse delay  $T_{rd}$  is given by:

### Equation 2

$$t_{rd} = 32 \times T_{osc}$$

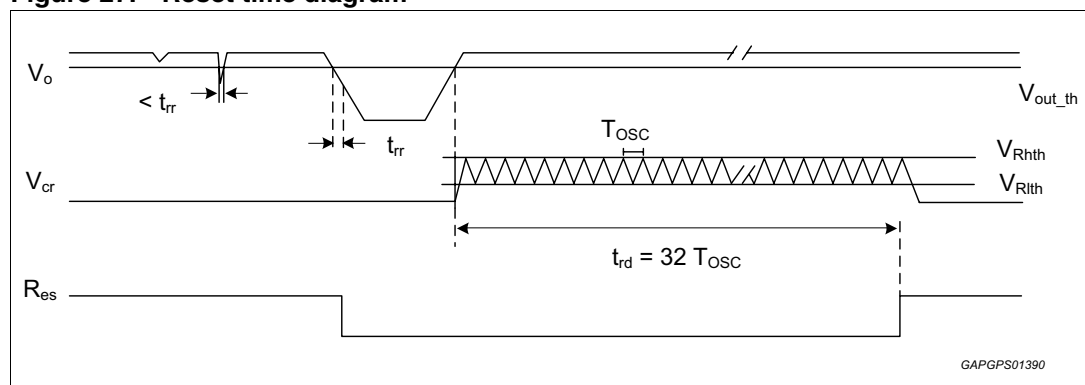
The Output Voltage Reset threshold can be adjusted via an external voltage divider  $R_1 + R_2$  ( $R_1$  connected between  $R_{es\_Adj}$  and  $V_0$ ,  $R_2$  connected between  $R_{es\_Adj}$  and GND) according to the following formula:

### Equation 3

$$V_{thre} = [(R_1 + R_2) / R_2] \times V_{Res\_adj}$$

The Output Voltage Reset threshold can be decreased down to 3.5 V. If it is needed to maintain it to its default value (8% below  $V_{o\_ref}$  typical), it is enough to connect the  $R_{es\_Adj}$  pin directly to GND.

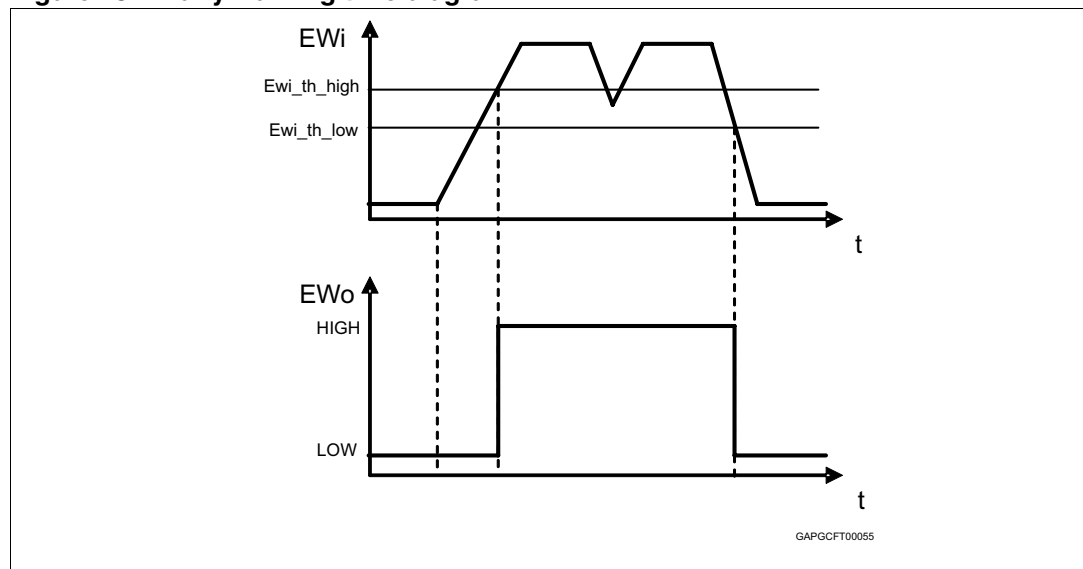
**Figure 27. Reset time diagram**



### 3.3 Early warning

This circuit compares the  $EW_i$  input signal with the internal voltage reference (typically 2.5 V). The use of an external voltage divider makes the comparator very flexible in the application. This function can be used to supervise the supply input voltage either before or after the protection diode and to give additional information to the microprocessor such as low voltage warnings.

**Figure 28. Early warning time diagram**



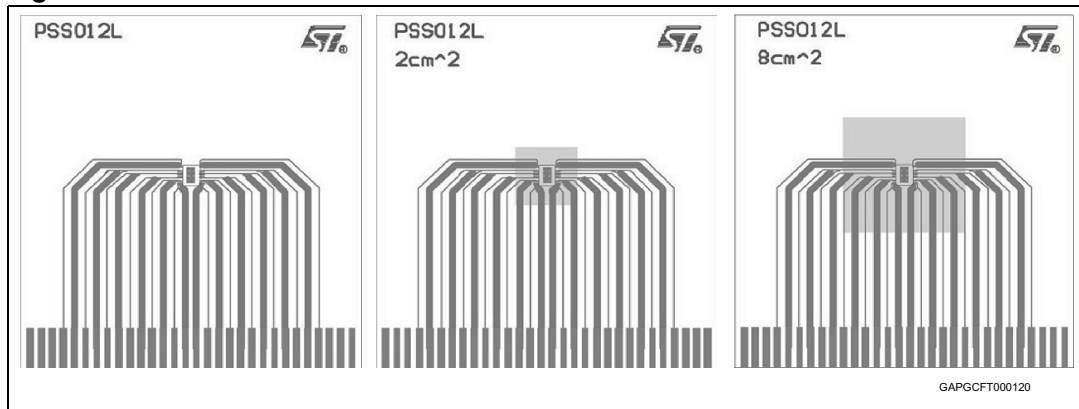
### 3.4 Enable

L5150GJ is also provided with an enable input, an high signal switches the regulator on. When the enable pin is set to low the output is switched-off and the current consumption of the device is 5  $\mu$ A typical.

## 4 Package and PCB thermal data

### 4.1 PowerSSO-12 thermal data

Figure 29. PowerSSO-12 PC board<sup>(1)</sup>



1. Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70  $\mu$ m (front and back side) thermal vias separation 1.2 mm, thermal via diameter 0.3 mm +/- 0.08 mm, Cu thickness on vias 25  $\mu$ m, footprint dimension 4.1 mm x 6.5 mm ).

Figure 30.  $R_{thj-amb}$  vs PCB copper area in open box free air condition

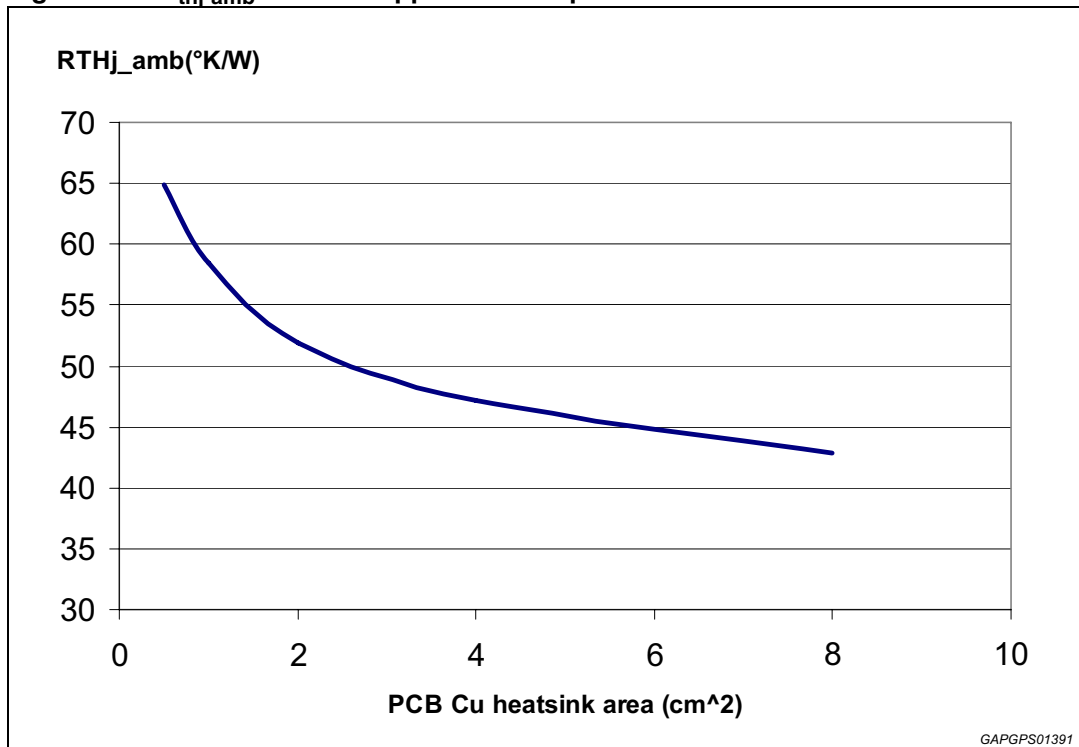
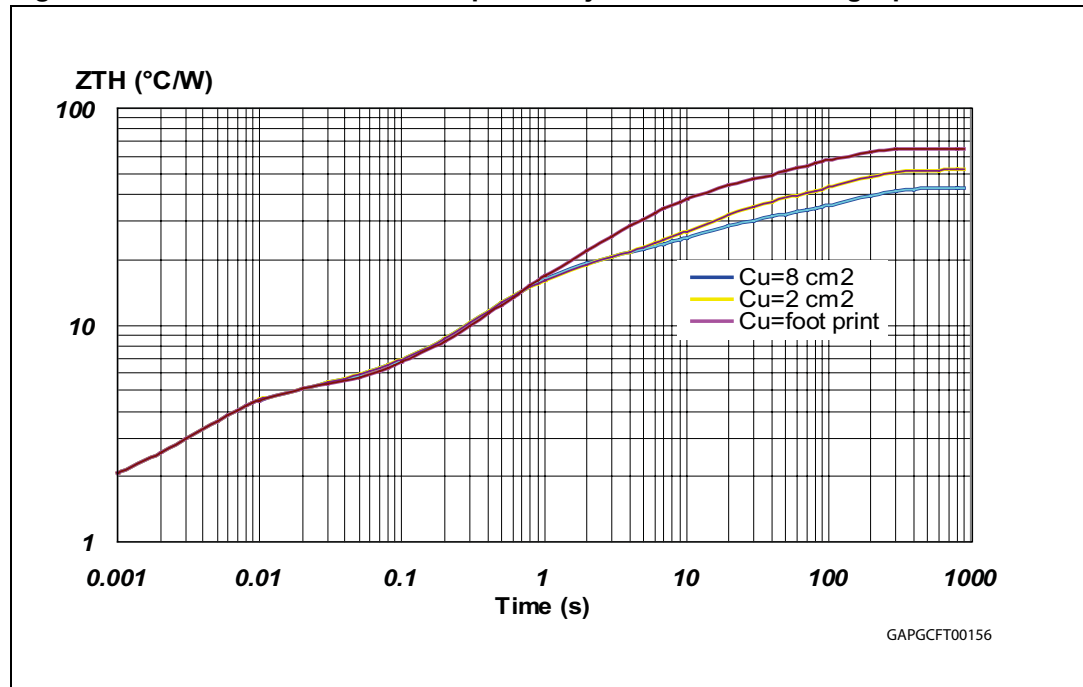


Figure 31. PowerSSO-12 thermal impedance junction ambient single pulse

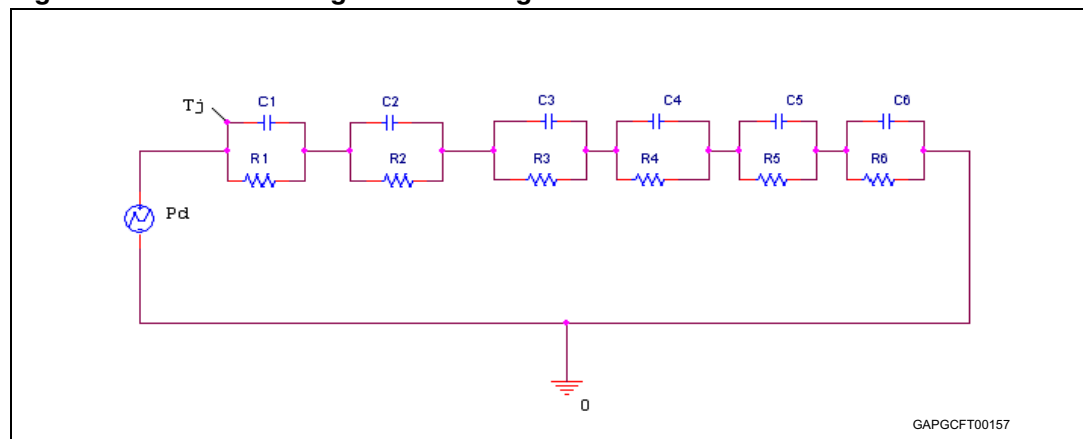


Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p/T$

Figure 32. Thermal fitting model of Vreg in PowerSSO-12



**Table 9. PowerSSO-12 thermal parameter**

Area (cm <sup>2</sup> )	Footprint	2	8
R1 (°K/W)	1.53		
R2 (°K/W)	3.21		
R3 (°K/W)	5.2		
R4 (°K/W)	7	7	8
R5 (°K/W)	22	15	10
R6 (°K/W)	26	20	15
C1 (W.s/°K)	0.00004		
C2 (W.s/°K)	0.0016		
C3 (W.s/°K)	0.08		
C4 (W.s/°K)	0.2	0.1	0.1
C5 (W.s/°K)	0.27	0.8	1
C6 (W.s/°K)	3	6	9

## 5 Package and packing information

### 5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 5.2 PowerSSO-12 mechanical data

Figure 33. PowerSSO-12 package dimensions

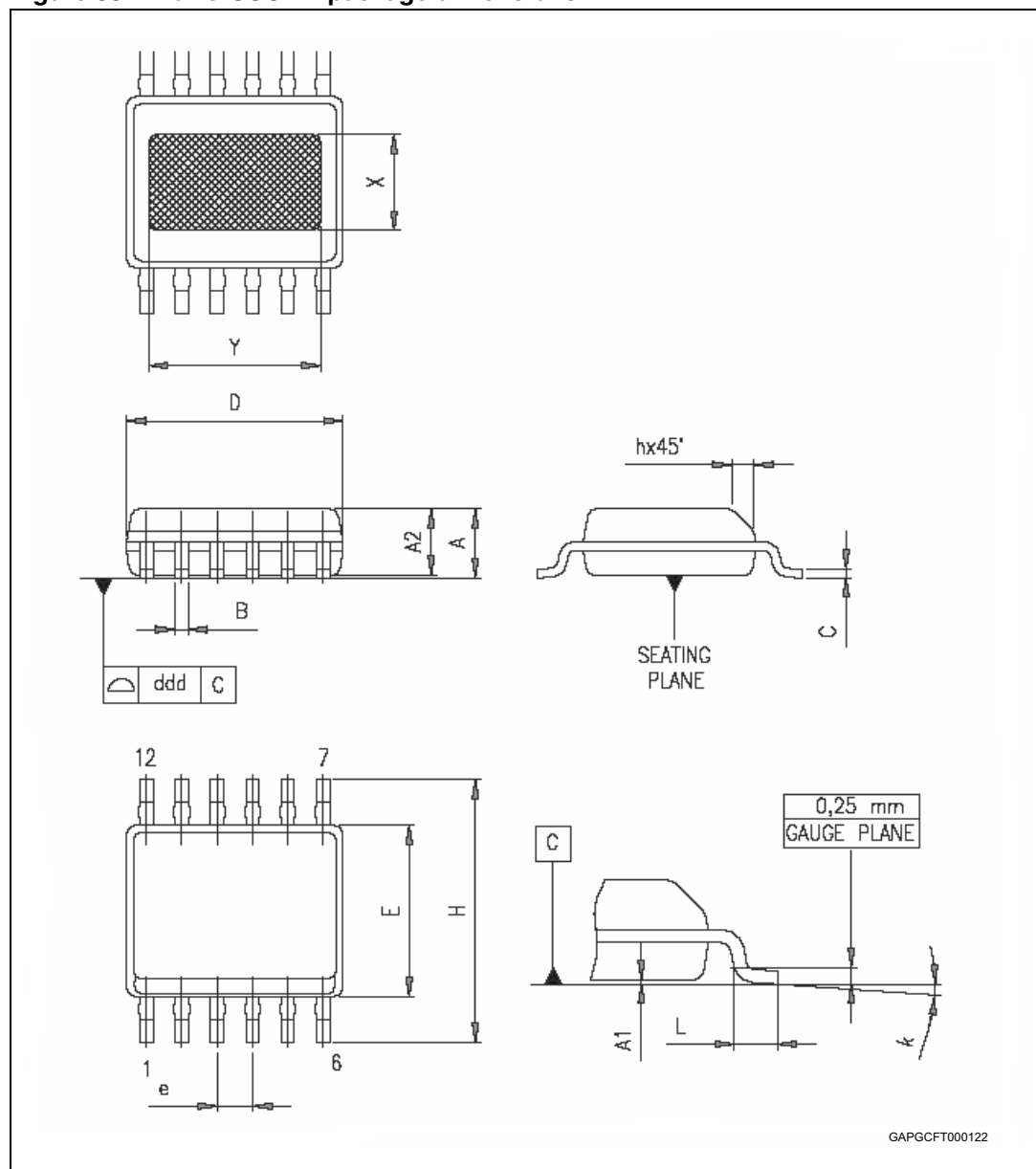


Table 10. PowerSSO-12 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
B	0.230		0.410
C	0.190		0.250
D	4.800		5.000
E	3.800		4.000
e		0.800	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0°		8°
X	1.900		2.500
Y	3.600		4.200
ddd			0.100



### 5.3 PowerSSO-12 packing information

Figure 34. PowerSSO-12 tube shipment (no suffix)

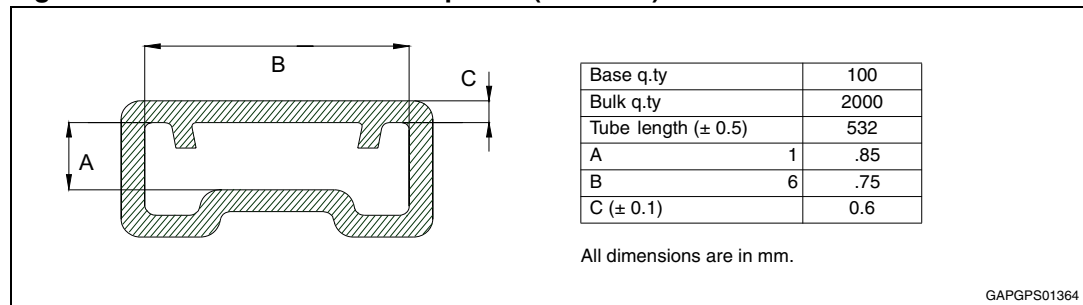
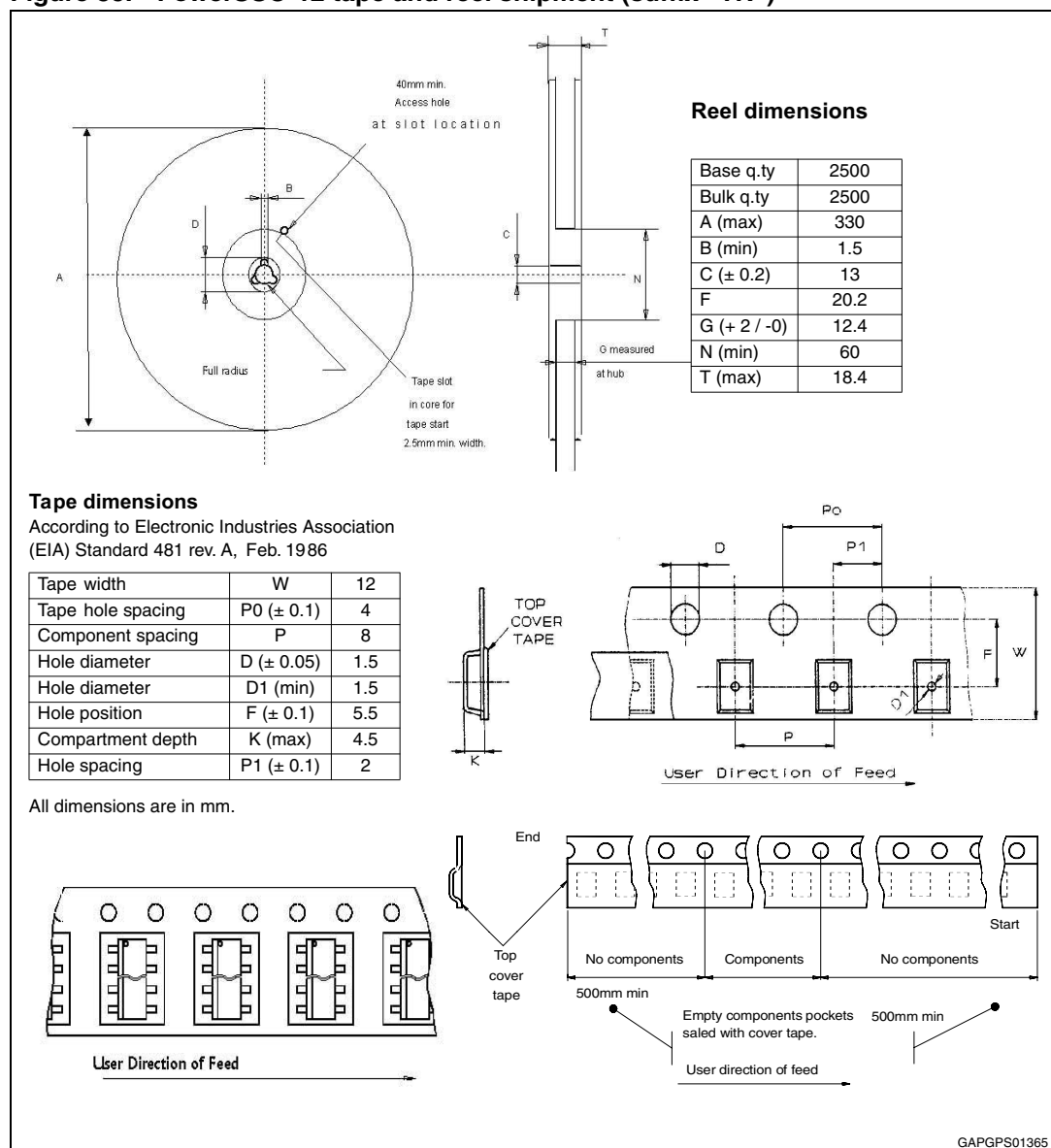


Figure 35. PowerSSO-12 tape and reel shipment (suffix "TR")



## 6 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
09-Aug-2007	1	Initial release.
06-Mar-2008	2	<p>Modified <a href="#">Description</a> on cover page.</p> <p>Updated <a href="#">Table 5.: General</a>:</p> <ul style="list-style-type: none"> <li>– changed <math>V_{O\_ref}</math>, <math>V_{line}</math>, <math>V_{load}</math> test conditions</li> <li>– added notes to <math>I_{lim}</math> and <math>V_{dp}</math> parameters</li> <li>– added <math>I_{oth\_H}</math>, <math>I_{oth\_L}</math>, <math>I_{oth}</math> parameters.</li> </ul> <p>Updated <a href="#">Table 6.: Reset</a>:</p> <ul style="list-style-type: none"> <li>– added <math>V_{Res\_adj}</math> parameter</li> <li>– changed <math>V_{Rlth}</math> values (min./ typ./ max.) from 17/20/23 to 20/23/26 (% <math>V_{O\_ref}</math>).</li> </ul> <p>Updated <a href="#">Table 8.: Enable</a>:</p> <ul style="list-style-type: none"> <li>– changed <math>V_{En\_hyst}</math> typ. value from 800 mV to 500 mV</li> <li>– changed <math>I_{leak}</math> typ. value from 3 <math>\mu A</math> to 1.8 <math>\mu A</math>.</li> </ul> <p>Modified <a href="#">Section 3.2: Reset</a>.</p>
09-May-2008	3	<p>Updated <a href="#">Table 5.: General</a> :</p> <ul style="list-style-type: none"> <li>– changed <math>I_{lim}</math> values (Min./Typ./Max.) from 0.7/1/1.30 A to 280/470/660 mA.</li> <li>– <math>V_{O\_ref}</math> parameter : updated <math>I_o</math> test condition Old -&gt; <math>I_o = 0.1</math> mA to 10mA New -&gt; <math>I_o = 0.1</math> mA to 8 mA.</li> </ul>
13-Oct-2008	4	<p>Updated <a href="#">Table 5.: General</a> :</p> <ul style="list-style-type: none"> <li>– <math>V_{load}</math> parameter : updated <math>I_o</math> test condition Old -&gt; <math>I_o = 5</math> mA to 150 mA New -&gt; <math>I_o = 8</math> mA to 150 mA</li> </ul>

Table 11. Document revision history (continued)

Date	Revision	Changes
15-Apr-2009	5	<p>Updated corporate template</p> <p>Updated <a href="#">Figure 2: Configuration diagram (top view)</a></p> <p><a href="#">Table 2: Pins description</a></p> <ul style="list-style-type: none"> <li>– Added new row</li> </ul> <p><a href="#">Table 4: Thermal data</a></p> <ul style="list-style-type: none"> <li>– <math>R_{thj-amb}</math>: changed value</li> <li>– Updated TableFootnote</li> </ul> <p><a href="#">Table 5: General</a></p> <ul style="list-style-type: none"> <li>– <math>V_{load}</math>: changed max value for <math>V_S = 8\text{ V}</math> to <math>18\text{ V}</math>, added new row</li> <li>– <math>I_{qn\_1}</math>: changed Test conditions (added <math>T_j = 25\text{ °C}</math>), added new row</li> </ul> <p><a href="#">Table 6: Reset</a></p> <ul style="list-style-type: none"> <li>– <math>V_{Rlth}</math>: changed min/typ/max value</li> <li>– <math>V_{Res\_adjl}</math>: replaced with <math>V_{Rlth}</math>, changed Parameter</li> </ul> <p><a href="#">Table 7: Early warning</a></p> <ul style="list-style-type: none"> <li>– Updated symbols</li> </ul> <p>Added <a href="#">Figure 3: Output voltage vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 4: Output voltage vs. <math>V_S</math></a></p> <p>Added <a href="#">Figure 5: Output voltage vs. <math>V_{En}</math></a></p> <p>Added <a href="#">Figure 6: Drop voltage vs. output current</a></p> <p>Added <a href="#">Figure 7: Current consumption vs. output current</a></p> <p>Added <a href="#">Figure 8: Current consumption vs. output current (at light load condition)</a></p> <p>Added <a href="#">Figure 9: Current consumption vs. input voltage (<math>I_o = 0.1\text{ mA}</math>)</a></p> <p>Added <a href="#">Figure 10: Current consumption vs. input voltage (<math>I_o = 75\text{ mA}</math>)</a></p> <p>Added <a href="#">Figure 11: Current limitation vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 12: Current limitation vs. input voltage</a></p> <p>Added <a href="#">Figure 13: Short-circuit current vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 14: Short-circuit current vs. input voltage</a></p> <p>Added <a href="#">Figure 15: <math>V_{En\_high}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 16: <math>V_{En\_low}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 17: <math>V_{Rhth}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 18: <math>V_{Rlth}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 19: <math>V_{EWi\_thh}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 20: <math>V_{EWi\_thl}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 21: <math>I_{cr}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 22: <math>I_{dr}</math> vs. <math>T_j</math></a></p> <p>Added <a href="#">Figure 23: PSRR</a></p> <p><a href="#">Section 3.1: Voltage regulator</a></p> <ul style="list-style-type: none"> <li>– Updated text</li> <li>– Added <a href="#">Figure 24: Application schematic</a></li> <li>– Added <a href="#">Figure 26: Maximum load variation response</a></li> </ul> <p><a href="#">Section 3.2: Reset</a></p> <ul style="list-style-type: none"> <li>– <math>V_{Rlth}</math>: changed value from <math>1.15\text{ V}</math> to <math>0.9\text{ V}</math> in <a href="#">Equation 1</a></li> </ul> <p>Updated <a href="#">Section 3.4: Enable</a></p> <p>Added <a href="#">Section 4: Package and PCB thermal data</a></p> <p>Changed <a href="#">Section 5.1: ECOPACK®</a></p>

Table 11. Document revision history (continued)

Date	Revision	Changes
09-Jun-2009	6	<p>Changed document title</p> <p><a href="#">Table 5: General</a></p> <p>– <math>I_{\text{oth\_H}}</math>, <math>I_{\text{oth\_L}}</math>: added test condition</p> <p>Updated <a href="#">Figure 4: Output voltage vs. <math>V_S</math></a></p> <p><a href="#">Section 3.3: Early warning</a></p> <p>– changed internal voltage reference typical value from 1.23 V to 2.5 V</p> <p>Updated <a href="#">Figure 31: PowerSSO-12 thermal impedance junction ambient single pulse</a></p>
04-Dec-2009	7	<p>Updated features list.</p> <p>Updated <a href="#">Table 2: Pins description</a>.</p> <p>Updated <a href="#">Section 3.1: Voltage regulator</a>.</p> <p>Corrected <a href="#">Equation 3</a> on <a href="#">Section 3.2: Reset</a>.</p>
19-Apr-2010	8	<p>Updated footnote description of <a href="#">Table 4: Thermal data</a>.</p> <p>Updated <a href="#">Figure 30: <math>R_{\text{thj-amb}}</math> vs PCB copper area in open box free air condition</a>.</p> <p>Updated <a href="#">Table 9: PowerSSO-12 thermal parameter</a>.</p>
30-Jan-2012	9	Updated <a href="#">Figure 25: Stability region on page 16</a> .
07-Feb-2012	10	Modified <a href="#">Figure 25: Stability region on page 16</a> .

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